IN THE CLAIMS

1. (Previously Presented) An electrostatic discharge (ESD) protection device comprising:

a substrate;

a first doped region formed in the substrate for connecting to a bonding pad; and

a second doped region formed in the substrate for connecting to a power node, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein the first and second doped regions are positioned such that current flows in one direction between the bonding pad and the power node through the substrate.

2. (Previously Presented) The ESD protection device of claim 1, wherein the substrate comprises a first conductivity type and the first and second doped regions comprise a second conductivity type.

3. (Previously Presented) The ESD protection device of claim 1, wherein the substrate comprises a p-type conductivity material and the first and second doped regions comprise an n-type conductivity material.

4. (Previously Presented) The ESD protection device of claim 1, wherein first and second doped regions comprise a higher doping concentration than a doping concentration of the substrate.

5. (Previously Presented) The ESD protection device of claim 1 further comprising a first isolation structure placed on an opposing side of the first doped region from a region separating the first and the second doped regions, and a second isolation structure placed on an opposing side of the second doped region from a region separating the first and the second doped regions.

6. (Previously Presented) An electrostatic discharge (ESD) protection device comprising:

a substrate;

a first doped region formed in the substrate for connecting to a bonding pad; and

a second doped region formed in the substrate for connecting to a power node, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the ESD protection device is structured such that an amount current flowing between the first and second doped regions is not controlled by a voltage potential of a gate above the first and second doped regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein the first and second doped regions are positioned such that current flows in one direction between the bonding pad and the power node through the substrate.

7. (Previously Presented) A gateless electrostatic discharge (ESD) protection device comprising:

a substrate;

a first doped region formed in the substrate for connecting to a bonding pad; and

a second doped region formed in the substrate for connecting to a power node for receiving a power source, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the gateless ESD protection device comprises no isolation structure between the first and second dope regions, and wherein the first and second doped regions are positioned such that current flows in one direction between the bonding pad and the power node through the substrate.

8. (Currently Amended) ~~An~~ The ESD protection device of claim 7 ~~comprising:~~

~~a substrate;~~

~~a first active region formed in the substrate; and~~

~~a second active region formed in the substrate and separated from the first active region by only the substrate region~~, wherein each of the first and second ~~active~~ doped regions includes a source/drain region, a LDD region and a halo region, wherein the LDD region surrounds the source/drain region and the halo region surrounds the LDD region~~, wherein the ESD protection device comprises no gate above the first and second active regions~~.

9. (Previously Presented) The ESD protection device of claim 8, wherein the substrate comprises a first conductivity type and the source/drain region comprises a second conductivity type.

10. (Previously Presented) The ESD protection device of claim 8, wherein the substrate comprises a p-type conductivity material and the source/drain region comprises an n-type conductivity material.

11. (Previously Presented) The ESD protection device of claim 9, wherein the LDD region comprises the same conductivity type as the conductivity type of the source/drain region, wherein a doping concentration of the LDD region is lower than a doping concentration of the source/drain region.

12. (Previously Presented) The ESD protection device of claim 9, wherein the halo region comprises the same conductivity type as the conductivity type of the substrate, wherein a doping concentration of the halo region is lower than a doping concentration of the substrate.

13. (Previously Presented) An electrostatic discharge (ESD) protection device comprising:

a substrate; and

an implant within the substrate, the implant including two implant regions spaced apart by only the substrate region, the two implant regions including a first implant region connected to a bonding pad, and a second implant region connected to a power node, wherein the substrate comprises a first conductivity type and the two implant regions comprise a second conductivity type, wherein the ESD protection device is structured such that a conductivity between the two implant regions is not controlled by voltage potential of a gate above the two implant regions, wherein the ESD protection device comprises no isolation structure between the first and second implant regions, and wherein the first and second implant regions are positioned such that current flows in one direction between the bonding pad and the power node through the substrate.

14. (Currently Amended) ~~An~~ The ESD protection device ~~comprising:~~

~~a substrate;~~ of claim 7, wherein the first and second doped regions are located in a first implant ~~a first implant within the substrate, the first implant including two first doped regions spaced apart by only the substrate region~~, wherein the first implant comprises a first depth[[;]] , wherein the ESD protection device further comprises a second implant inside the two first doped regions, the second implant comprising a second depth, wherein the second depth is shallower than the first depth; and

a third implant inside the second implant, the third implant comprising a third depth, wherein the third depth is shallower than the second depth, and wherein the ESD protection device comprises no gate above the first, second and third implants.

15. (Currently Amended) ~~An~~ The ESD protection device ~~comprising:~~ of claim 7, wherein the first doped region includes a first active region and the second doped region includes a second doped region,

~~a substrate;~~

~~a first active region formed in the substrate; and~~

~~a second active region formed in the substrate and separated from the first active region by only the substrate region,~~ wherein each of the first and second active regions includes a source/drain region, wherein the first active region further includes an LDD region and a halo region, and wherein the LDD region surrounds the source/drain region and the halo region surrounds the LDD region~~, wherein the ESD protection device comprises no gate above the first and second active regions~~.

16. (Currently Amended) ~~An~~ The ESD protection device ~~comprising:~~ of claim 7, wherein the first doped region includes a first active region and the second doped region includes a second doped region,

~~a substrate;~~

~~a first active region formed in the substrate; and~~

~~a second active region formed in the substrate and separated from the first active region by only~~

~~the substrate region,~~ wherein the first active region includes an LDD region surrounded by a halo region [[,]] and an ohmic-contact region adjacent to the halo region, wherein the second active region include a source/drain region~~, wherein the ESD protection device comprises no gate above the first and second active regions~~.

17. (Previously Presented) An integrated circuit comprising:

a voltage source;

an external bonding pad; and

an electrostatic discharge (ESD) protection device connected between the external bonding pad and the voltage source, the ESD protection device comprising:

a substrate;

a first doped region formed in the substrate and connected to the external bonding pad; and

a second doped region formed in the substrate and connected to the voltage source, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein the first and second doped regions are positioned such that current flows in one direction between the external bonding pad and the voltage source through the substrate.

18. (Previously Presented) The ESD protection device of claim 17, wherein the substrate comprises a first conductivity type and the first and second doped regions comprise a second conductivity type.

19. (Previously Presented) The ESD protection device of claim 17, wherein the substrate comprises a p-type conductivity material and the first and second doped regions comprise an n-type conductivity material.

20. (Previously Presented) The ESD protection device of claim 17, wherein first and second doped regions comprise a higher doping concentration than a doping concentration of the substrate.

21. (Previously Presented) The integrated circuit of claim 17, wherein the voltage source is connected to ground.

22. (Previously Presented) The integrated circuit of claim 17, wherein the voltage source is connected to a voltage supply.

23. (Previously Presented) An integrated circuit comprising:

a first voltage source;

a second voltage source;

an external bonding pad;

a first electrostatic discharge (ESD) protection device connected between the first voltage source and the external bonding pad; and

a second ESD protection device connected between the second voltage source and the external bonding pad, wherein the second ESD protection device comprising:

a substrate;

a first doped region formed in the substrate and connected to the external bonding pad; and

a second doped region formed in the substrate and connected to the second voltage source, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the second ESD protection device comprises no gate above the first and second doped regions, wherein the second ESD protection device comprises no isolation structure between the first and second dope regions, and the first and second doped regions are positioned such that current flows in one direction between the external bonding pad and the second voltage source through the substrate.

24. (Previously Presented) The integrated circuit of claim 23, wherein the first voltage source is substantially smaller than the second voltage source.

25. (Previously Presented) The integrated circuit of claim 23, wherein the first voltage source is connected to ground.

26. (Previously Presented) The integrated circuit of claim 23, wherein the second voltage source is connected to a voltage supply.

27. (Previously Presented) An integrated circuit comprising:

a voltage source;

an external bonding pad;

an internal circuit connected to the external bonding pad at a node; and

an electrostatic discharge (ESD) protection device connected between the node and the voltage source, the ESD protection device comprising:

a substrate;

a first doped region formed in the substrate and connected to the external bonding pad; and

a second doped region formed in the substrate and connected to the voltage source, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein the first and second doped regions are positioned such that current flows in one direction between the external bonding pad and the voltage source through the substrate.

28. (Previously Presented) An integrated circuit comprising:

a first voltage source;

a second voltage source;

an external bonding pad;

an internal circuit connected to the external bonding pad at a node;

a first electrostatic discharge (ESD) protection device connected between the first voltage source and the node; and

a second ESD protection device connected between the second voltage source and the node, wherein the second ESD protection device comprising:

a substrate;

a first doped region formed in the substrate and connected to the external bonding pad; and

a second doped region formed in the substrate and connected to the second voltage source, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the second ESD protection device comprises no gate above the first and second doped regions, wherein the second ESD protection device comprises no isolation structure between the first and second dope regions, and wherein the first and second doped regions are positioned such that current flows in one direction between the external bonding pad and the second voltage source through the substrate.

29. (Previously Presented) A semiconductor chip comprising:

a package having a plurality of pins; and

an electrostatic discharge (ESD) protection device connected to at least one of the pins, the protection device comprising:

a substrate;

a first doped region formed in the substrate for connecting to the at least one of the pins; and

a second doped region formed in the substrate for connecting to a power node, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the ESD protection device comprises no gate above the first and second doped regions, wherein the ESD protection device comprises no isolation structure between the first and second dope regions, and wherein the first and second doped regions are positioned such that current flows in one direction between the at least one of the pins and the power node through the substrate.

30-32. (Canceled)

33. (Previously Presented) A chip comprising:

a package having a plurality of pins; and

a protection device connected to at least one of the pins, the protection device comprising:

a substrate;

a first doped region formed in the substrate and connected to the at least one of the pins; and

a second doped region formed in the substrate for connecting to a power node, wherein the second doped region is separated from the first doped region by only the substrate region, wherein the protection device comprises no isolation structure between the first and second dope regions, and wherein the first and second doped regions are positioned such that current flows in one direction between the at least one of the pins and the power node through the substrate.

34. (Previously Presented) A chip comprising:

a package having a plurality of pins; and

a protection device connected to at least one of the pins, the protection device comprising:

a substrate; and

an implant within the substrate, the implant including two implant regions spaced apart by only the substrate region, the two implant regions including a first implant region connected to the at least one of the pins, and a second implant region connected to a power node, wherein the substrate comprises a first conductivity type and the two implant regions comprise a second conductivity type, wherein the protection device is structured such that a conductivity between the two implant regions is not controlled by voltage potential of a gate above the two implant regions, wherein the protection device comprises no isolation structure between the first and second implant regions, and wherein the first and second doped regions are positioned such

that current flows in one direction between the bonding pad and the power node through the substrate.

35. (Previously Presented) A chip comprising:

a package having a plurality of pins; and

a protection device connected to at least one of the pins, the protection device comprising:

a substrate;

a first doped region formed in the substrate and connected to the at least one of the pins; and

a second doped region formed in the substrate for connecting to a power node, wherein the second doped region is separated from the first doped region by only the substrate region such that an amount current flowing between the first and second doped regions is not controlled by a voltage potential of a gate above the first and second doped regions, wherein the protection device comprises no isolation structure between the first and second dope regions, and wherein the first and second doped regions are positioned such that current flows in one direction between the at least one of the pins and the power node through the substrate.

36. (Previously Presented) A circuit comprising:

a bonding pad;

a power node; and

a transistor connected between the bonding pad and the power node, the transistor including a substrate, a first doped region formed in the substrate, and a second doped region formed in the substrate, the transistor including no gate above the first and second doped regions, the transistor including no isolation structure between the first and second doped regions, the first doped region connecting to the bonding pad, the second doped region connecting to the power node, wherein the first and second doped regions are positioned such that current flows in one direction between the bonding pad and the power node through the transistor.

37. (Previously Presented) The circuit of claim 36, wherein the substrate includes a first conductivity type material and each of the first and second doped regions includes a second conductivity type material.

38. (Previously Presented) The circuit of claim 36, wherein the substrate includes a p-type conductivity material and each of the first and second doped regions includes an n-type conductivity material.

39. (Previously Presented) The circuit of claim 36 further comprising a first isolation structure formed next to the first doped region, and a second isolation structure formed next to the second doped region.